REMARKS

In response to the Office Action, Applicant respectfully requests the Examiner to reconsider the above-captioned application in view of the foregoing amendments and the following comments.

Discussion of Claim Rejections Under 35 U.S.C. § 103(a)

In the Office Action, the Examiner rejected Claims 1, 2, 4-12, 14-16, 18-26, 28-49 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,914,727, to Horan (hereinafter "Horan"), et al. in view of U.S. Patent No. 5,869,101, to Arimilli, et al. (hereinafter "Arimilli") and U.S. Patent No. 4,718,006 to Nishida. Claims 3 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Horan, Arimilli, and Nishida in view of U.S. Patent No. 6,002,411, to Dye. Claims 13 and 27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Horan, Arimilli, and Nishida in view of U.S. Patent No. 6,118,462, to Margulis (hereinafter "Margulis"). Claim 50 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Horan, Arimilli, Margulis, Nishida, and Dye.

Claims 1, 14, 28, and 40

Applicant respectfully disagrees with these rejections. To establish a *prima facie* case of obviousness a three-prong test must be met. First, there must be some suggestion or motivation, either in the references or in the knowledge generally available among those of ordinary skill in the art, to modify the reference. Second, there must be a reasonable expectation of success found in the prior art. Third, the prior art reference must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991). Applicant respectfully submits that there is no motivation to combine the references as suggested by the Examiner and that the cited references, even if combined, fail to describe or suggest all of the claimed limitations.

Horan is generally directed to a system for providing a logic chipset that functions between a bridge and a memory controller. In Horan, a central processing unit 102 is connected to a core logic chipset 204 through a memory bus 204. *See* Horan, col. 10, lines 47-49. As was recognized by the Examiner in the Office Action, Horan describes a single controller for controlling the main memory, i.e., memory interface and control 304. In the Office Action, the

Examiner relied upon Arimilli as teaching the usage of two memory controllers for controlling a main memory.

In response, Applicant acknowledges that Arimilli uses two memory controllers for controlling memory; however, Applicant respectfully submits that it does not use memory controllers as is presently claimed. For example, Claim 1, as amended recites: "wherein each of the at least two memory controllers is configured to communicates with a central processing unit via the central processing unit bus [and] wherein each memory controllers are independent of the processor." Arimilli describes a symmetric multiprocessor system comprising multiple partial system memories 18a-18n and corresponding memory controllers 17a-17n. In Arimilli, each of the CPUs *incorporates* a memory controller 17b. *See* Figure 2 and col. 2, lines 6-8. In Arimilli, each of the memory controllers do not communicate with the processor via the system bus (24), see Figure 2. Thus, in Arimilli, each of the CPUs (21a-21n) do not communicate with each of their associated CPUs via a central processing unit bus, as is claimed.

Furthermore, Applicant respectfully submits that in Arimilli, the memory controllers are not independent of the processor, as is claimed. Arimilli teaches that a memory controller should not be connected to the system bus but instead to be integrated within the CPU. *See* Figure 1 (prior art) and Figure 2A. As is seen from Figure 2, each of the memory controllers are incorporated within the CPU. Thus, Applicant respectfully submits that if Horan was modified by Arimilli, such combination would not derive the claimed invention. Such combination would have a fundamentally different architecture. Such combination would not result in a system "wherein each of the at least two memory controllers is configured to communicate with a central processing unit via the central processing unit bus, wherein each memory controllers are independent of the processor."

Further this feature is neither taught nor suggested in the other references. In particular, in the Office Action, the Examiner relied upon Margulis as teaching "an enhanced [integrated] system controller 310 connected to [various devices including an advanced graphics port (AGP)334]." *Id.* at 8. The Examiner further relied upon Dye as teaching "an integrated memory controller comprising a single chip and including two memory control units for providing interface signals to communicate with respective banks of the system memory." *Id.* at 9. Thus, Applicant submits that the cited references, either individually or combination, fail to teach or suggest, at least, the above-limitations, and all claims are in condition to be allowed.

Claims 2-13, 15-27, 29-39, and 41-50

Since Claims 2-13, 15-27, 29-39, and 41-50, each depend on one of Claims 1, 14, 28, and 40, Applicant respectfully submits that these claims are allowable for at least the reasons discussed above and the subject matter of their own limitations.

Summary

Applicant has endeavored to address all of the Examiner's concerns as expressed in the outstanding Office Action. In light of the above amendments and remarks, reconsideration and withdrawal of the outstanding rejections is respectfully requested. If the Examiner has any questions which may be answered by telephone, he is invited to call the undersigned directly.

Respectfully submitted,

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